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Study of electromigration-induced formation of discrete voids in flip-chip solder joints by in-situ 3D laminography observation and finite-element modeling

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ABSTRACT

In the microelectronics industry the flip-chip (FC) technology is broadly used to enhance the packaging density. However, the small size and the unique geometry of the FC solder joints induce the electromigration (EM) reliability issue. In this study, a pair of lead-free solder joints (SAC1205) was EM tested by a current of 7.5 × 10^7 A/cm². During the tests, X-ray laminography was applied to observe the microstructure evolution in-situ. Laminography enables the non-destructive observation of the bump microstructure and allows for a quantitative three-dimensional (3D) analysis. After EM testing for 650 h, a new EM failure mechanism was found, differing from the two well-known models, the pancake void propagation and the under-bump-metallization dissolution. Here, a few pre-existing small voids grew and simultaneously many new voids formed and grew over the entire EM testing period. Most of the nucleating voids were distributed in the current crowding region, a few also located in the low-current-density region. As the testing time increased, voids increasingly coalesced with each other, forming a porous network which occupied a large part of the interface area and caused the EM failure. A finite-element (FE) method was then applied to analyze the interplay between the microstructure evolution and current density redistribution. A series of 3D FE models was built based on the laminography images for the different testing stages. The current density distribution from the FE analysis indicates that the formation of discrete voids did not affect the global current density distribution until a major coalescence of the voids occurred. The relieving of the global current crowding in the pancake void model was not found in this new EM failure mechanism. It was the local current crowding around individual void found in the new mechanism that is held responsible for the EM retardation.

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1. Introduction

In the past decades, the microelectronics industry put the miniaturization of electronic devices at the top priority and has advanced steadily, but nowadays approaching the end of Moore’s law [1–3], the shrinkage pace of the semiconductor devices is slowing down. In order to meet the demand for higher device density and performance, the industry has investigated the future route of combining chip technology and packaging technology, and as a result various packaging techniques have been developed. Among them, the flip-chip (FC) solder joint is essential because it uses area arrays of a large number of solder joints to conduct the signals and therefore dramatically rises the bandwidth [4,5]. However, the small size and unique geometry of FC joints induce reliability issues such as electromigration (EM) and current crowding effects [6–9]. Two main failure mechanisms of EM have been reported: void propagation [6–7,10–12] and under-bump-

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metallization (UBM) dissolution [13–17]. To observe the microstructure evolution, however, the samples were cross-sectioned and polished to the desired interface before the EM tests [17–20]. This made the observed failure interface to be a free surface, which is an infinite vacancy source. Furthermore, the free surface causes oxidation, releases the accumulation of stress, and significantly affects the heat dissipation. To avoid the influence of such sample treatment and to obtain reliable three-dimensional (3D) data, synchrotron X-ray laminography (SRCL) [21] was applied to non-destructively observe void formation in this study. Moreover, in order to understand the current density distribution change with the microstructure evolution, a series of finite-element (FE) models was built reflecting the 3D microstructure observed at the different stages of the EM testing.

The combination of 3D imaging technique and FE methods has already been applied to geo-materials and bio-materials [22–29]. N. Chawla and R. S. Sidhu used a serial sectioning method to obtain the 3D microstructure [22–26]. The image quality of the reconstructed 3D microstructure generally was affected by the polishing depth control and the polishing quality, and the samples cannot be tested after imaging. Instead of the serial sectioning method, P.G. Young et al. applied computed micro-tomography (CT) to obtain the 3D images of the desired objects [27]. Although the resolution of micro-CT is sufficient for the observation of bones or minerals, it is not particularly suited to the observation of microelectronic devices where modified CT approaches have been investigated [30]. This is due to the measurement geometry which leads to the missing information for extended flat-plate-like objects [31] such as (assembled) printed-circuit boards. For such objects, laminographic imaging techniques turn out more adapted [32–34]. Laminography using laboratory sources have presently been used to characterize ball-grid arrays and other large interconnect types [35] but usually struggle when it comes to flip-chip interconnects due to the limited spatial resolution. Here synchrotron laminography can be adapted to a wide variety of interconnect types [36].

From the viewpoint of FE modeling, C. M. Tsai constructed a two-dimensional FE model which involves the initial pattern of the solder bump before EM testing [37]. His purpose was to correlate the current density and the displacement of the Pb particles to obtain the product of diffusivity and effective charge number (DZ) of Sn. However, the atomic diffusion driven by EM was 3D, which was difficult to present in a 2D model. Furthermore, the microstructure evolved simultaneously during EM testing. As a result, the simple model that constructed only according to the initial pattern was unable to properly describe the ensuing changes.

In this study, we applied SRCL to trace the microstructure evolution stage-by-stage during the EM testing. We combined 3D imaging and constructed the FE models according to the acquired 3D images. This approach shows several advantages. SRCL provides high-quality and high-resolution images, which are well suited to inspect the structural components of a variety of flat objects such as plant leaves [38], fossils [39], cracks inside plate-shaped engineering materials [40–43], or solder joints in microelectronic devices [34,44–47]. In the present study we use it to observe the formation of numerous discrete voids and their growth during the EM testing. In particular, the laminography technique is able to image the microstructure without any destruction, unlike the aforementioned in-situ scanning electron microscopy (SEM) [17–20]. As a result, the test environment of the sample was similar to the real ambient of usage and maintained the same in the different stages of testing. This allowed us also in contrast to previous studies to keep a stage-by-stage tracing of the microstructure evolution during testing [48,49]. Since FE models were constructed according to the 3D images in different EM testing stages, the interaction between the current density distribution and the microstructure evolution during testing could be well examined.

To summarize, lead-free solder bumps were EM tested by a high current density for several hundreds of hours, and were imaged by SRCL at different EM stages. The experimental results from the reconstructed laminographic 3D images allowed for revealing and quantifying the void formation at associated EM testing stages. As a consequence, a series of finite element model could be derived from these 3D images so as to examine the correlation between the void formation and the current density distribution.

2. Experimental and methods

2.1. Materials and EM tests

For the EM tests in this study, we adopted a single printed circuit board with 4 identical wafer-level chip-scale-packaging test chips provided by National Semiconductor Corporation. The dimension of one chip was 3000 μ m × 3000 μ m and there were 36 solder balls on a chip [48]. The solder was a lead-free solder type SAC1205, consisting of Sn, Ag (1.2%), Cu (0.5%), and Ni (0.05%). A constant 2.5 A current was applied for up to 830 h to one selected chip, and the current flowed only through one pair of the bumps in the chip, resulting in a current density of 7.5 × 10^3 A/cm² on the UBM opening. During current stressing, a furnace and a thermocouple were also used to set and monitor the surface temperature of the chip to 130 °C. The sample structure is illustrated in Fig. 1. The diameters of passivation opening and UBM opening were 210 μ m and 270 μ m, respectively, and the bump height was 220 μ m. The top trace was 1 μ m thick Al. The top UBM was 7.5 μ m thick Ti/Cu/Cu layer and the bottom trace was Cu. These materials provide good adhesion on the top and bottom surface of the solder. According to the direction of electron flow, the left solder that experienced a downward electron flow was labeled as Bump 1, and the right one with the opposite flow direction was labeled as Bump 2. Because the top trace is much thinner than the bottom trace, the damage caused by EM is expected to be more severe in Bump 1 than in Bump 2 [50,51]. Therefore, in particular, the top interface of Bump 1 where a high flux of electrons entered was our major region of interest (ROI) (Fig. 1(a)).

2.2. In-situ 3D laminography observation

In order to observe the electromigration in-situ, non-destructive observation by 3D synchrotron X-ray computed laminography imaging was applied to the afore-described flip-chip specimen. The experiment was performed at the beamline ID15A [52] of the European Synchrotron Radiation Facility (ESRF) in Grenoble, France, and the general setup is illustrated in Fig. 1(c–d). Details of the experimental technique and sample setup employed are given in Refs. [21,53,54], especially in Fig. 2(b) of Ref. [54]. We used a laminographic axis inclination angle of about 25° (θ = 65°) and filtered white beam illumination. The solder bumps at their initial state (0 h) were first scanned by laminography before the EM tests were started. Then the EM testing protocol was applied. Once the EM testing reached certain stages, the current stressing was temporarily stopped, and the sample was scanned by laminography again. For each scan, the sample was mounted on a rotary stage and continuously rotated by 360° in the X-ray beam, where 1999 angularly equidistant projections of 1024 × 1024 pixels were collected using an indirect CCD-based detector system [55]. The exposure time of each projection was 600 ms. The effective pixel size of the detector was 0.84 μ m, resulting in a field of view (FOV) of 0.86 mm × 0.86 mm. Finally, the 3D volumes of the solderers at different EM stages were reconstructed using a filtered back-projection algorithm [56]. Following the time sequence of EM
testing, in-situ 3D non-destructive observation of the microstructure evolution in flip-chip solder joints was achieved. After EM testing, the sample was also polished for SEM observations (the polished cross-section is indicated by the dashed line in Fig. 1(b)).

3D image analysis was subsequently applied to the reconstructed data. The 3D images reveal microstructural information concerning the void properties and growth. In addition, these 3D experimental volumes were used for constructing finite element models so as to find out the current density redistribution due to the void formation.

2.3. Finite element modeling

In order to build the 3D FE models directly from the obtained 3D experimental volumes, some additional post-processing steps were needed on the laminography images, which are summarized in Fig. 2. (1) The 3D volumes of different EM stage have to be well aligned to the same position in order to trace the microstructure evolution. (2) Different materials in terms of voids and solder matrix were segmented by a grey-level thresholding method, and the segmented elements were labeled, forming the binarized 3D images of models. The systematic error [57] of these image analyses was estimated to be around ±1.4–2% for all dataset. (3) The 3D binarized volumes were then converted voxel by voxel into the format of a finite element model. (4) Since the entire solder as a global model was computationally too consuming, a submodel method was applied. (5) In this method, global models were built first with large elements ignoring some details. (6) Then the global models were solved with proper boundary conditions (2.5 A at 130 °C). (7) Submodels containing only the ROI that is the top 50 μm of the solder and UBM where the most severe EM damage occurred were built with fine elements. (8) Accordingly, the boundary conditions of the submodels were interpolated from the results of the global models. (9) Finally, the submodels (ROI) were solved, and the results of current density distribution were extracted.

The complete working flow of combined in-situ laminography and FE analysis is summarized in Fig. 3.
3. Result and discussion

Figure 4 shows the backscattered electron (BSE) microscopic images from SEM characterization after EM testing and polishing. They are compared to the reconstructed laminography cross-sections in side and plane view of Bump 1 and Bump 2 after the final EM testing stage for 650 h, respectively. From the BSE images (Fig. 4(a1–e2)), a few small voids were observed at the UBM/solder interface. The artifacts introduced by polishing can be clearly seen (the many granule-like features on the solder surface). In comparison, SRCL allows for inspecting the ROI in three dimensions, and we see from Fig. 4(c1) that in fact there was intensive void formation at the interface of Bump 1. This demonstrates the advantage of laminography that direct 3D observation can give rich information on EM-induced void formation at the interface of Bump 1. This demonstrates the advantage of laminography that direct 3D observation can give rich information on EM-induced void formation, which is hardly gained on 2D surfaces. However, it should also be pointed out that the resolution of SRCL is inferior to BSE imaging as the thin UBM layer and the intermetallic compound (IMC) formation can hardly be resolved in SRCL. Therefore, in the later FE model, the initial thickness of the remaining UBM and IMC were assumed as 5.0 μm and 3.5 μm respectively, presuming the 2.5 μm thick UBM was consumed during the sample fabrication and the reaction followed the mass conservation law.

Figure 4(c1–c2) and (e1–e2) reveal that the void formation in Bump 2 was significantly less pronounced than in Bump 1, this can be explained with the fact that the top interface is the anode end for Bump 2, where the TM-induced flux was in the opposite direction of the EM-induced flux [50,51] hence leading to a reduced effect of void growth here compared to that of Bump 1. Therefore, in the following we will focus on the SRCL results of Bump 1 where the electromigration dominated the failure of the solder joints.

Figure 5 presents the void evolution during EM testing in Bump 1. Unlike the pancake-type void growth mechanism observed in previous studies, a different EM failure mechanism was found here. It can be clearly identified that a considerable number of discrete voids nucleated and grew independently at the UBM/solder interface in Bump 1 of interest. Especially, after 78 h the voids tended to form more intensively in the vicinity of the current crowding spot. This microstructure evolution is important because it may considerably change the consequent local current density distribution during the EM testing.

Resorting to 3D imaging analysis, quantitative information of void growth can be extracted. Figure 6(a) reports the total volume of voids and the void growth rate (the latter is equal to the change of total void volume per testing time duration). The total volume of voids steadily increased with the testing time. However after 100 h of EM testing, the void growth rate dropped by over 50% from 957.1 μm³/h (at 108.0 h) to 444.5 μm³/h (at 303.0 h). It is worth mentioning that in Fig. 6(a), the change of the total volume of voids as a function of time resembles an “S” curve in the Johnson-Mehl-Avrami’s theory of phase transformation. It is slow in the beginning due to low nucleation rate, and then in the later stage it slows down again due to heavy impingement of voids which will reduce both nucleation and growth.

Together considering the evolution of the number of voids versus stressing time shown in Fig. 6(b), the void growth mechanism can be divided into two stages. Stage I: before 108.0 h, void nucleation and growth were the dominant phenomena; Stage II: after 108.0 h, voids grew by cross-linking and impingement. In addition, there was a sharp increment in void number from 42 to 159 at the beginning of the test which indicates that in spite of the pre-existing voids, EM still caused the nucleation/growth of voids.

![Fig. 3. The entire EM testing and observation workflow.](image-url)

![Fig. 4. (a) Backscattered electron (BSE) microscopic images after EM testing and polishing; (b) the 2D cross-sections of reconstructed 3D laminography data (in side view); and (c) the 2D cross-sections in plane view at the UBM/solder interface of reconstructed laminography data of the Bump 1 and Bump 2 after EM testing for 650 h. (The voids are dark and the solder is close to white. The dashed lines in (b) and (c) indicate the location of the orthogonal views with respect to each other.) The projection of all interfacial voids onto the plane of the UBM opening at (d) the initial stage (0 h) and (e) the late stage (540.3 h) of the EM testing allow one to distinguish pre-existing voids.](image-url)
multiple voids at the interface. The average volume of voids continued to increase through the entire test although the increasing rate of the average volume slowed down after 100 h of testing. These two curves in Fig. 6(b) may indicate two facts: 1. The merging and cross-linking of voids continuously happened after 47 h of the entire EM testing; 2. The rate of void cross-linking was slightly higher than the rate of new void formation in stage II.

Fig. 6(c) contains further evidence of the change of void growth mechanism. The total area of voids was measured by the complete area of voids projected onto the plane of the UBM opening, and the average thickness of voids was obtained from the division of the total volume of voids by the projected area of voids. As the figure shows, the average thickness of voids increased from 2.90 μm (at 13.0 h) to 5.49 μm (at 108.0 h) and then maintained at about 6 μm after 108 h. This inferred that the volume increase of voids in the beginning 100 h was coming from the formation and isotropic growth of new voids. The increase of the average void volume after 100 h was coming predominantly from the lateral growth and the coalescence of voids.

The discrete voids growth and propagation mechanism observed in this study can be more clearly illustrated by plotting the projection of voids onto the plane of UBM opening as shown in Fig. 7. Before the EM testing time reached 90 h, new void formation could still be found in the projections (Fig. 7(a1–a10)). Even though new voids were continuously formed during the entire testing time period, it is clear that the formation of individual new voids was the dominant microstructure evolution in the first 100 h of EM testing. After EM testing for 47 h, some void coalescence started to appear. After 90 h testing, the merges and cross-linking between voids became the major effect. Figure 7(c) is a composite picture of Fig. 7(a1–a10). The red and yellow regions indicate the voids forming in the early stages of EM testing; the green, blue, and purple regions indicate the voids forming in the late stages. Pointed out by the arrows in Fig. 7(c), the green and blue regions between the red and yellow ones correspond to the coalescence zones between voids.

By evaluating the void volume distributions, we are able to retrieve the movement of the center of mass of those growing voids. From Fig. 8(a), we observed that the most favorable site for void growth moved towards the current crowding point (-X direction) during stage I, where it remained similarly during stage II.
In Fig. 8(b), the observed shift of the void mass center in X and Y directions lead to the conclusion that in stage I, voids developed more independently in 3 dimensions and mostly at pre-existing defects, whilst in the later stage II, the dominant mechanism was in-plane void growth leading to void coalescence mainly close to the global crowding zone and the final appearance of larger flat voids. Unlike the pancake-type void, the discrete voids here tended to move globally (center of mass) and locally (see Fig. 7(c)) towards the current crowding zone and not away from it. We will go into greater detail about this in the subsequent FE analysis.

Through the 3D FE models built according to the laminography images, the correlation between the microstructure evolution and the corresponding current density distribution at each EM stage becomes clearer and the 3D failure mechanism can be better interpreted. One example is shown in Fig. 9, the ROI of Bump 1 after 540 h testing was simulated. Figure 9(a1–a7) were the laminography images at different observation planes (indicated in Fig. 9(e)). After the alignment, the images were segmented to obtain 3D images suited as input of the model (Fig. 9(b1–b7)), and then further meshed into the FE models (Fig. 9(c1–c7)) to calculate the current density distribution during EM testing (Fig. 9(d1–d7)). The observation positions marked from 1 to 7 are noted in Fig. 9(e), which is the bottom layer of the UBM. The discrete voids due to the EM testing were resolved clearly between the top UBM and the solder. These voids significantly affected and redistributed the current density near the current crowding spot, which is the entrance point of the electron flow. The distortions induced the local current crowding around the discrete voids, which will be discussed in detail in the following paragraphs. The discrete voids affected the current density distribution in a different way than the pancake-type void does. In order to compare, the conventional pancake void model was also simulated in this study and illustrated in 2D in Fig. 10 and in 3D in Fig. 11(a), respectively. As shown in Fig. 10, once the pancake-type void is formed, the void blocks the current penetration. Then as the void propagates, the current detours through a longer path and accumulates along the tip of the pancake-type void. As a result, the original current crowding region is shifted along the growing path of the pancake void and the associated EM gets slightly relieved because the larger void spreads the crowded current onto a longer edge. However at the same time, the longer route of current flow causes a higher heat generation. This extra heat generation might enhance the effects of electromigration and thermomigration. The mechanism of the pancake-type void development is also illustrated in 3D by the FE simulation in Fig. 11(a). The pancake void changes the current crowding region from the edge of UBM opening to the front edge of the propagating void. In contrast, the discrete voids found in this study did not change the global current density distribution significantly during the void formation in EM testing as shown in Fig. 11(b). Although the discrete voids caused the local redistribution of current density, the remaining solder between different voids still allowed the passage of current and maintained the global current density distribution rather similar to the initial state.

The current density distribution found at different stages of EM testing gives evidence of this phenomenon, too. Figure 12(a–d) represents the central cross-sections of the laminography images, segmented 3D images, FE models, the current density distributions of the Bump 1’s ROI, respectively, and their evolution with the EM testing time. In the microstructure development of column (a), discrete voids formed near the global current crowding region and grew individually as the EM testing time increased. After long time testing, the voids coalesced with each other and then became large.
planar voids, which caused the EM failure. Therefore, the driving mechanism for EM failure observed in this study differs from the ones described in the literature, although at the late stages the coalescence yields some large and flat voids at the IMC/solder interface and also, the UBM dissolution was observed, as can be seen from the BSE image in Fig. 4(a).

During the stage of void coalescence (Stage II), the void growth rate considerably decreased (Fig. 6(a)), and this could be explained through the current density distribution obtained by FE analysis. In Fig. 13, the current density distribution close to the global current crowding region is displayed in magnified views for four selected stages. It is shown that the global current density marked by the dashed curve did not significantly change with the testing time. However, the formation of new voids caused a local current crowding around the voids. Because a void blocked the electron flow, the electron flow had to split and bypass the void. As a result, low current density regions were established at the front and the back of the void, and high current density regions formed on the two sides of the void with respect to the direction of electron flow. This local current crowding around individual voids also spread the current onto a larger area and relieved the impact of EM during the test. The global current crowding is inherently related to the sample geometry. In the case of the pancake-type void, the growth and propagation of the void can spread the current from crowding in a small spot onto an elongated edge around the void to relieve the EM [58,59]. This also happened in the case of the discrete voids. Although the discrete voids did not change the global current crowding phenomenon, the discrete voids induced local current crowding and provided much longer edges around the voids. The locally high current density at the two sides of the void promoted the depletion of solder, and thus the void continued to grow and coalesce with adjacent voids at the later stages of EM. Consequently, the void growth rate maintained at a relatively stable range of values in the beginning (Stage I, Fig. 6(a)) and then slowed down

![Fig. 8](image8.png) The evolution of the center of mass of the voids (a) in X direction and (b) in XY direction with respect to the EM testing sequence. The coordinate system is indicated in the inset image.

![Fig. 9](image9.png) (a1–a7) The laminography images in different cross-sectional planes corresponding to the dashed lines indicated in (e); (b1–b7) the segmented 3D image as input to the model; (c1–c7) the 3D FE models; and (d1–d7) the current density distribution of the ROI of Bump 1 at different observation planes after 540 h EM testing.
in the late stage (Stage II) of testing.

Let us recall the data in Fig. 7, when we virtually partition the projection of the solder cross-section into uniform columns (vertical stripes as indicated in Fig. 14(a)), a histogram representing the probability for the formation of new voids $P_r$ can be determined between each stage. The $P_r$ equals the number of elements changing from solder into void at the current stage divided by the total number of solder element in the previous stage of test. As an example, Fig. 14(a) plots the $P_r$ histogram from stage 103 h–108 h as a function of the horizontal coordinate. It is evidenced that at the global current crowding spot, new void formation or coalescence between voids possess the highest probability to happen compared to other regions.

According to the above observations, the correlation between the void propagation and the current density distribution should be discussed by two different viewpoints. From the viewpoint of the global current density distribution, the high current density induced higher opportunities for the voids to nucleate and grow as shown in Fig. 14(a). The correlation coefficient between the probability of void growth and the current density in solder was determined to be 0.673, in Fig. 14(b). This indicated that the EM was the dominant failure mechanism although the thermo-migration may also take place at the same time during the EM testing. On the contrary, the discrete void formation and growth did not affect the global current density distribution until the major coalescence between voids occurred. Once the coalescence caused the voids...
little current crowding near the interface between the IMC layer and the solder. Furthermore, if we assume heterogeneous nucleation of voids is easy at the IMC/solder interface, a large number of voids will form. Then the continuous nucleation and growth of these voids under EM and their impingement will lead to the behavior reported here.

4. Conclusions

A methodology to non-destructively measure the effects of electromigration induced damage mechanisms in solder/UBM material systems was introduced. It is based on combining in-situ 3D synchrotron radiation computed laminography (to image the microstructure in its natural environment) with FE analysis to determine current densities from the microstructure in order to elucidate the effects of current crowding. First results were presented for the widely-used lead-free SAC1205 solder and Ti/Cu/Cu UBM combination.

For this system, a new failure mechanism was discovered: the nucleation and growth of discrete voids which consecutively agglomerate to form very large voids. From the quantitative analysis of the obtained 3D volumes, we found that the EM-induced damage evolution can be divided into two stages. (I) At the beginning of EM testing (before 108.0 h), individual small discrete voids formed and grew at the UBM/solder interface. (II) Then in the later stage of testing (from 108.0 h onwards), those voids coalesced and cross-linked with each other, forming larger flat voids. Unlike the pancake-type void mechanism, the discrete voids nucleated at random positions of the interface, not only near the global current crowding spot but more scattered although the global current crowding spot was still the most favorable site for the void formation. From the 3D FE analysis, we found that these discrete voids did not alter the maximum global current density distribution as the pancake-type void does—the global current crowding phenomenon stayed similarly in the EM test (i.e. up to 503 h) before intense coalescence took place near the current entrance point. However, the local current crowding effect (induced by the individual voids) made the voids also tend to grow along the electron flow direction (like the pancake void behaves), and consequently also relieved the EM. This explains why the measured void growth rate maintained at a similar value in the early stage I while slowing down in the late stage II of the EM testing. Finally, the possible origin of this newly observed failure model was discussed.

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