Conventional n-channel MOSFET devices using single layer HfO_2 and ZrO_2 as high-k gate dielectrics with polysilicon gate electrode

Yudong Kim, Gabriel Gebara, Michael Freiler, Joel Barnett, Deborah Riley, Jerry Chen, Kenneth Torres, JaeEun Lim, Brendan Foran, Fred Shaapur, Avinash Agarwal, Patrick Lysaght, George A. Brown, Chadwin Young, Swarnal Borthakur, Hong-Jyh Li, Billy Nguyen, Peter Zeitzoff, Gennadi Bersuker, David Derro, Renate Bergmann, Robert W. Murto, Alex Hou, Howard R. Huff, [1]Eric Shero, [1]Christophe Pomarede, [1]Michael Givens, [1]Mike Mazanec, and [1]Chris Werkhoven

International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, U.S.A.
[1]ASM America, Inc., 3440 East University Drive, Phoenix, AZ 85034, U.S.A.

Abstract

Conventional self-aligned MOSFET transistors with poly-silicon gate-electrode were successfully fabricated using Hf-oxide and Zr-oxide as high-k gate-dielectrics. The gate-stack consisting of poly-silicon on Hf-oxide exhibited promising transistor characteristics with a S/D RTA temperature of 1000°C, demonstrating feasibility of integrating high-k gate-dielectrics into conventional CMOS process technology. Effects of S/D RTA temperatures on the HfO_2/Poly-Si transistor characteristics were discussed. A gate-dimension dependent bi-modal gate leakage current was observed from ZrO_2/Poly-Si transistors.

Introduction

High-k dielectric films are anticipated to be required as early as 2005 for certain applications with low power and leakage current specifications. Compatibility of the high-k materials with conventional industry standard MOSFET process flows using a poly-Si gate electrode and a thermal budget up to 1000°C is critical for the successful introduction of high-k films. In this work, conventional self-aligned planar n-channel MOSFET transistors with a poly-Si gate electrode were successfully fabricated using single layer HfO_2 and ZrO_2 as high-k gate dielectrics deposited by the ALD (Atomic Layer Deposition) method (1). This was accomplished with 200 mm production-worthy equipment with HfO_2 and with a process flow comparable with the ITRS 180 nm technology node (2). The high-k gate stack, consisting of poly-Si on HfO_2, exhibited promising transistor characteristics such as drive current, sub-V_t slope, and effective mobility equivalent to 85% of SiO_2, with a S/D RTA temperature of 1000°C for 10 sec, suggesting that the high-k gate dielectric film can be integrated into conventional self-aligned process technologies with minimal perturbations.

Process flow and experiments

A synopsis for the conventional high-k transistor process flow is illustrated in Figure 1. Surface preparation was done with an SC1/SC2 wet clean process prior to the ALD deposition of 5 nm ZrO_2 and 3 nm HfO_2 (physical thickness target). 200 nm thick amorphous Si was deposited on top of the high-k films using an LPCVD furnace process. Subsequent processing steps follow a typical self-aligned MOSFET process flow. The high-k films were successfully removed by a modified spacer etch recipe without impacting Ti-salicide performance. S/D RTA splits at 1000°C/10sec, 900°C/10sec, and 850°C/30sec were performed to evaluate the effect of the anneal temperatures on the high-k gate stack and transistor characteristics.

Results and discussion

A. ZrO_2/Poly-Si high-k transistors

The high-k transistor output characteristics with ZrO_2 are illustrated in Figure 2. V_t was around 1.5V, consistent with the presence of negative charges that can be annealed during S/D anneal as seen from the HfO_2/Poly-Si transistors. Drive current was accordingly reduced when compared to that of oxide baseline wafers. Figure 3 shows a bi-modal characteristic observed in the gate leakage currents: namely, transistors with L_{Drawn} of 0.5 micron or smaller showed ~1 mA/cm^2 of gate leakage, whereas transistors with L_{Drawn} at 1 micron or larger showed as high as $1x10^3$ A/cm^2 of gate leakage. The bi-modal gate leakage is hypothesized to be related to a gate dimension dependent Zr-silicide formation based on a metal-silicide formation model (3). The leakage prevents an EOT estimate by CV for ZrO_2 dielectric films; an HR-TEM of the gate dielectric is shown in Figure 4.

A variant on the hot H_2SO_4 wet etch process post gate-patterning was evaluated as an alternative to the spacer etch approach in removing ZrO_2. Excessive gate leakage currents were observed for all L_{Drawn} dimensions and Si structural defects at the gate edge were revealed by TEM as shown in Figure 5. The cause of the Si structural defect, either by the hot H_2SO_4 process or by other integration issues, has not yet been determined.

B. HfO_2/Poly-Si high-k transistors

The high-k transistors with HfO_2 demonstrated significantly improved transistor characteristics when compared to ZrO_2 as shown in Figure 6. Overall, HfO_2/Poly-Si transistor structure is shown in Figure 7 featuring Ti-salicide atop Poly-Si and in S/D regions, oxide spacer, HfO_2 layer beneath the oxide spacer, and the sub-oxide underneath HfO_2 in the spacer region. The sub-oxide growth is not surprising for ZrO_2 and HfO_2 when they are exposed to the ambient with a sufficient oxygen partial pressure (4).

The 1000°C S/D anneal has been shown to improve various capacitor and transistor characteristics such as CV behavior, EOT (equivalent oxide thickness), sub-V_t slope, and g_m when compared to the lower S/D anneal temperature

splits as shown in Figures 8 and 9. The poly-depletion effect became severe in the CV curves when the S/D anneal was done below 1000°C. EOT of 1.7 nm was extracted from 20/20 micron transistors with the 1000°C anneal split; overall, k of ~10.6 for the entire dielectric stack was obtained taking the total stack of 4.6 nm shown in Figure 10a after completing transistor processing. Table 1 summarizes EOT versus S/D RTA temperatures along with other physical characteristics. HR-TEM in Figure 10a showed ~ 0.4 nm thick bottom interfacial layer that is believed to be SiO_x or SiO_x doped with Hf. The chemical oxide from SC1/SC2 clean has been observed to reduce it's thickness from ~ 1 nm post HfO_2 deposition to ~ 0.5 nm post amorphous-Si deposition. The 1000°C sample exhibited a clearly defined and distinctive top interfacial layer when compared to the 850°C sample (Figure 10b). The HfO_2 thickness appeared to be reduced by 2 nm indicating either "densification of HfO_2" or "consumption by interacting with Poly-Si" upon higher temperature S/D anneal, although wafer-to-wafer thickness variations may not be ruled out.

Effective mobility as a function of effective electric field exhibited an approximately 15% reduction in peak mobility from the 1000°C anneal split when compared to the oxide control wafers as shown in Figure 11 (5). The peak mobility of 270 cm^2/V-sec is comparable to the ~230 cm^2/V-sec reported recently (6).

Gate leakage measured at 1.8V from transistors with W/L of 20/20 microns increased when the S/D anneal temperature increased as illustrated in Figure 12. The leakage level is acceptable at ~35 mA/cm^2 from the 1000°C, 10 second anneal split. As the EOT decreases with the increase in S/D RTA temperature (Table 1), the gate leakage current is expected to increase accordingly. Also, HfO_2 is anticipated to become more crystalline upon annealing at a higher temperature, resulting in more grain boundaries, possibly increasing the gate leakage current.

The HfO_2 high-k transistors exhibited a fairly high V_t when compared to that from the 4.5 nm SiO_2 baseline at International SEMATECH as shown in Figure 13. A simple V_t model indicated that the high V_t corresponded to the existence of negative charge of approximately $5x10^{12}/cm^2$ for 850°C and 900°C S/D RTA splits. The 1000°C anneal split suggested that the negative charge could be reduced to ~ $2x10^{12}/cm^2$. The level of negative charge observed in this work is consistent with other results with ALD high-k films (7). An "inverse" V_t roll-off behavior from the HfO_2/Poly-Si transistors is apparent in Figure 13. The inverse V_t roll-off behavior can be attributed to the sub-oxide growth resulting in bird's beak encroachment toward the channel region as shown in Figure 14. When channel length scales, the impact of the beak regions to V_t is expected to be more significant, rendering a V_t increase.

Figure 15 showed the transistor drive current dependency on the S/D anneal temperatures; the 1000°C split exhibited the best drive current. The suppressed drive current compared to the 4.5 nm SiO_2 baseline can be explained by the combined effect of the higher V_t and higher LDD resistance, R_x. The inverse Vt roll-off behavior also resulted in a lesser increase in the drive current for shorter L_{Drawn} devices. Arsenic LDD implant energy for the high-k transistors was increased, considering the remaining HfO_2 film in the LDD regions but was not high enough to account for the additional thickness increase due to the sub-oxide growth. Saturation current modeling with R_x indicated that R_x may be as high as 1.5x the SiO_2 baseline.

I_{OFF} remains constant below 100 pA/micron down to L_{Drawn} of 0.175 micron channel length as shown in Figure 16. This may be of advantage for the HfO_2/Poly-Si transistors to maintain reasonable I_{OFF} when L_{Drawn} scales.

Conclusions

Conventional self-aligned MOSFETs were successfully fabricated using ALD ZrO_2 and HfO_2 as gate dielectrics and poly-silicon gate electrode on a production-worthy planar Si-process technology. Overall transistor characteristics were better for HfO_2/Poly-Si transistors than ZrO_2/Poly-Si transistors. HfO_2/Poly-Si transistors demonstrated promising characteristics with a S/D anneal cycle at 1000°C for 10 seconds. Mobility degradation was estimated to be ~ 15% for HfO_2/Poly-Si transistors when compared to that from SiO_2 control wafers. Inverse V_t roll-off behavior was evident and process optimization will be necessary to improve the V_t and drive current of the HfO_2/Poly-Si transistors. A gate-dimension dependent bi-modal gate leakage current was observed from ZrO_2/Poly-Si transistors.

References

1) M. Tuominen et al., High-k Oxides by Atomic Layer Chemical Vapour Deposition, *Rapid Thermal Processing and Other Short-Time Processing Technologies I*, ECS **PV 2000-9**, 271-282 (2000).
2) Semiconductor Industry Association International, International Technology Roadmap for Semiconductors (2000).
3) C. Hobbs et al., Sub-Quarter Micron Si-Gate CMOS with ZrO_2 Gate Dielectric, VLSI-TSA, 204-207 (2001).
4) D. Wicaksana et al., Lanthanium and Zirconium Oxides for Alternative High Permittivity Gate Dielectrics, MRS Spring Meeting, 2001, MRS 670, Abstr. No. K.1.7 (to be published).
5) J. R. Hauser and K. Ahmed, Characterization of Ultra-Thin Oxide Using Electrical CV and IV measurements, Characterization and Metrology for ULSI Technology, p. 235, 1998.
6) S. J. Lee et al., Performance and Reliability of Ultra Thin CVD HfO_2 Gate Dielectrics with Dual Poly-Si Gate Electrodes, 2001 Symposium on VLSI Technology, p. 133, 2001.
7) M. Houssa et al., Variation in the fixed charge density of SiO_x/ZrO_2 gate dielectric stacks during post-deposition oxidation, Appl. Phys. Lett., 77, p.1885, 2000.
8) K. Chen et al., The impact of device scaling and power supply change on CMOS gate performance, EDL 17, No.5, p.202, May 1996.

Table 1. Comparison between 1000°C/10sec and 850°C/30sec RTA splits. BI: bottom interface, TI: top interface, and k is the overall k for the total dielectric stack, all in nm.

	BI	HfO2	TI	Total	EOT	k
1000C 10 sec	0.4	3.7	0.5	4.6	1.7	10.6
850C 30 sec	0.4	5.7	0.8	6.9	3.0	9.0

- 200 mm, (100), p/p+ epitaxial wafer
- Poly buffered LOCOS + well formation/channel-implants
- HF-dip + SC1/SC2 wet clean
- ALD of either ZrO_2 or HfO_2
- Amorphous Si dep + Phosphorus ion implant
- Gate patterning:
  - Split: Hot H_2SO_4 wet etching of ZrO_2 post-gate patterning
- LDD implant + Spacer deposition
- Spacer etch: Modified spacer etch to remove ZrO_2 or HfO_2
- SD implant + RTA anneal
  - Split: 1000°C/10sec, 900°C/10sec, 850°C/30sec
- Ti-salicide formation
- ILD deposition + CMP planarization
- Contact W-plug formation
- Metal deposition and patterning
- FG anneal

Figure 1. Synopsis of process flow

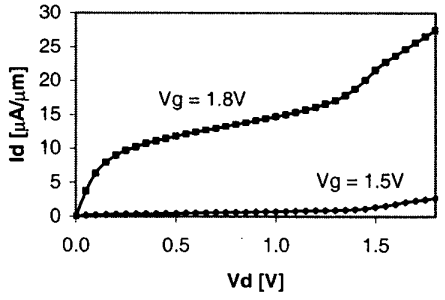

Figure 2. Transistor Id-Vd characteristics of a ZrO_2/Poly-Si transistor. W/L = 10/0.15 micron; S/D RTA anneal at 900°C for 10 seconds.

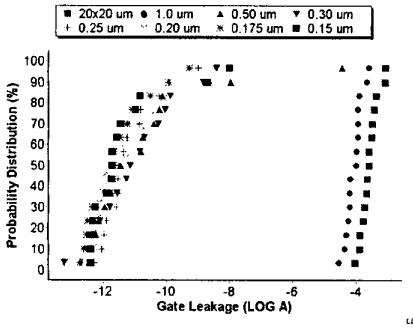

Figure 3. Bi-modal gate leakage current measured at 1.8V from ZrO_2/Poly-Si transistors. W=10 micron except W/L of 20/20 micron devices.

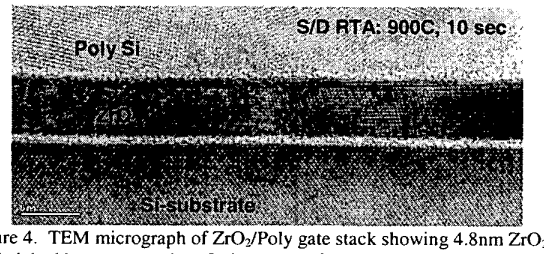

Figure 4. TEM micrograph of ZrO_2/Poly gate stack showing 4.8nm ZrO_2 sandwiched between two interfacial layers of 1.1nm each.

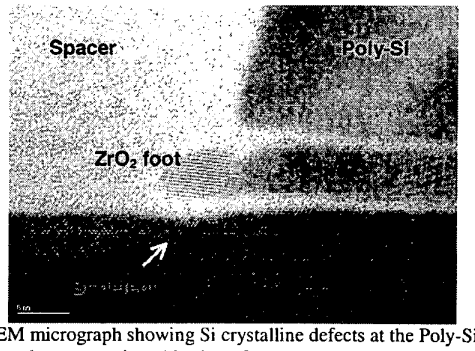

Figure 5. TEM micrograph showing Si crystalline defects at the Poly-Si gate edge after complete processing. No sign of gate-undercut was observed.

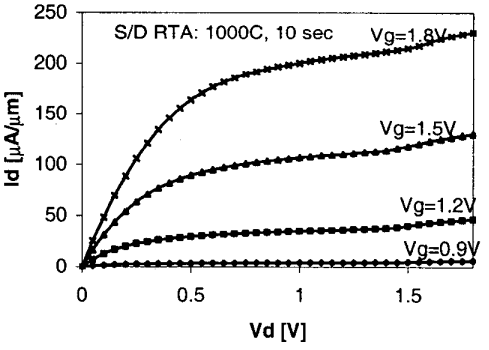

Figure 6. Transistor Id-Vd characteristics from a HfO_2/Poly transistor with W/L = 10/0.15 microns.

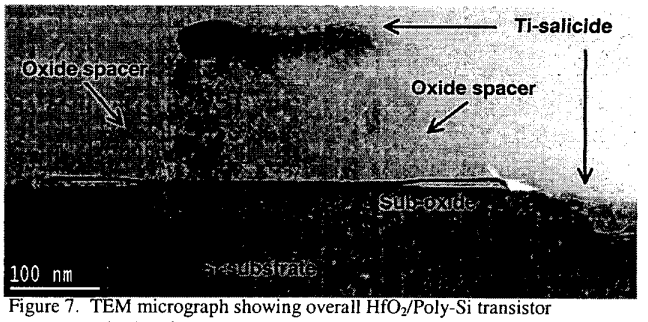

Figure 7. TEM micrograph showing overall HfO_2/Poly-Si transistor structure and sub-oxide growth underneath HfO_2 in the spacer region.

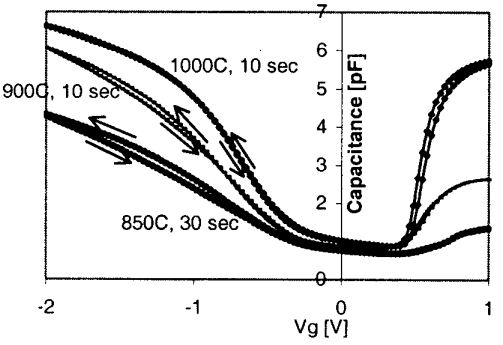

Figure 8. CV curves (100 KHz) collected from W/L of 20/20 micron HfO_2/Poly-Si transistors.

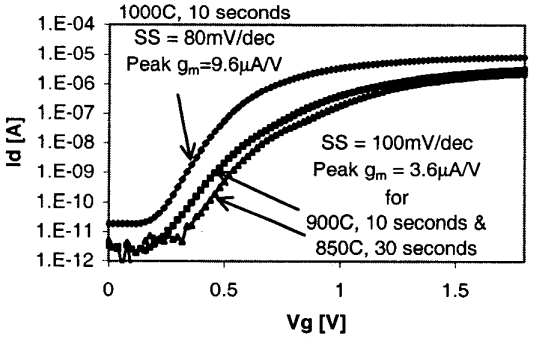

Figure 9. Sub-Vt slope and peak g_m measured from W/L = 20/20 micron HfO_2/Poly-Si transistors. Vd = 50mV.

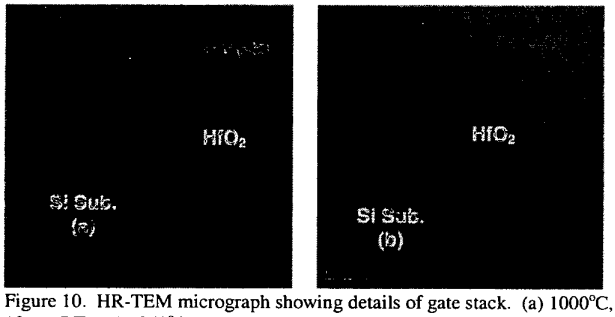

Figure 10. HR-TEM micrograph showing details of gate stack. (a) 1000°C, 10 sec RTA, (b) 850°C, 30 sec RTA.

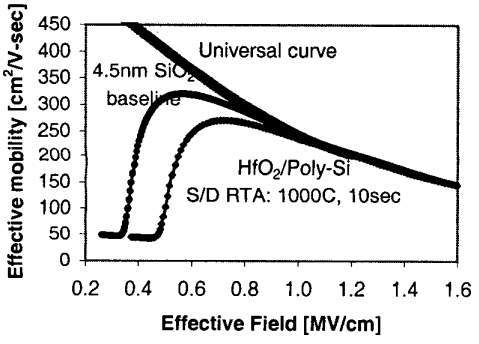

Figure 11. Effective mobility vs. effective field from HfO_2/Poly-Si transistor compared to that of oxide baseline. Universal curve from Chen et al. (8).

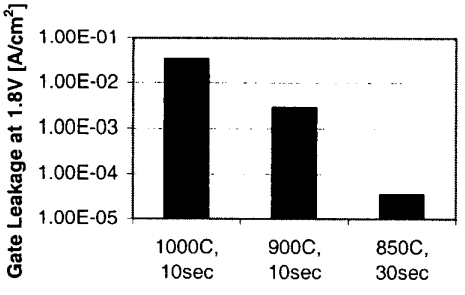

Figure 12 Gate leakage current density observed from W/L = 20/20 micron HfO_2/Poly-Si transistors as a function of S/D RTA conditions.

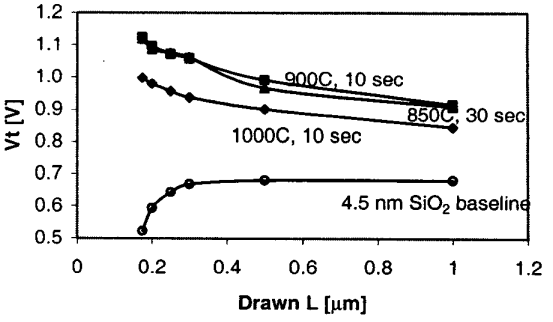

Figure 13. Threshold voltage trend as a function of transistor L drawn.

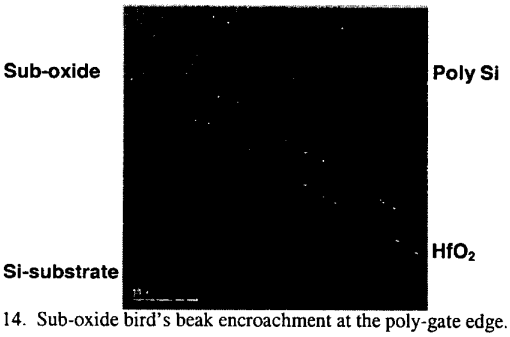

Figure 14. Sub-oxide bird's beak encroachment at the poly-gate edge.

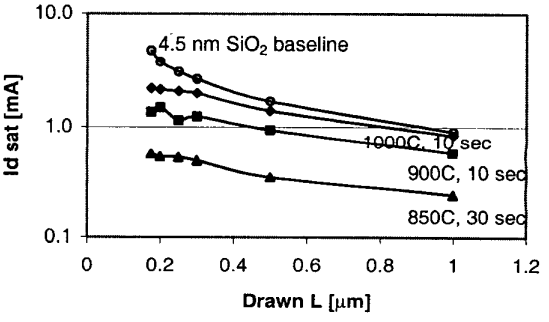

Figure 15. Drive current trend as a function of transistor L drawn. W is 10 micron for all devices. 4.5 nm SiO_2 baseline is the reference.

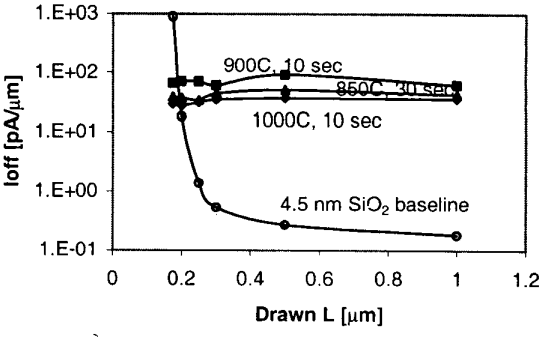

Figure 16. I_{OFF} measured at 1.8V as a function of transistor L drawn.