To Optimize Electrical Properties of the Ultrathin (1.6 nm) Nitride/Oxide Gate Stacks With Bottom Oxide Materials and Post-Deposition Treatment

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Abstract—The electrical properties affected by the bottom oxide materials and the post-deposition treatment on the ultrathin (down to 1.6 nm) nitride/oxide (N/O) stacks, prepared by rapid thermal chemical vapor deposition (RTCVD) with two-step NH3/N2O post-deposition annealing, for deep submicrometer dual-gate MOSFETs have been studied extensively. N/O stack with NO-grown bottom oxide exhibits fewer flat-band voltage shifts and higher hole and electron mobility, but suffers from worse leakage current than that with conventional O2-grown bottom oxide. In post-deposition treatment, increasing NH3 nitridation temperature can effectively reduce the equivalent oxide thickness (EOT) and improve leakage current reduction rate, but it can result in worse mobility. Furthermore, the subsequent N2O annealing eliminates the defects and offers a contrary effect on the N/O stack in comparison with the NH3 nitridation step.

Index Terms—Bottom oxide, N2O, NH3, nitride/oxide (N/O), post-deposition annealing, ultrathin.

I. INTRODUCTION

FOLLOWING the continuous down-scaling of devices, the conventional silicon dioxide cannot be applied as the ultrathin gate dielectric in the near future for ultra-large-scale integration (ULSI) CMOS technology. This is because the direct tunneling in ultrathin (<2 nm) oxide film causes an exponential increase in gate leakage current with decreasing oxide thickness [1], [2]. For example, gate leakage current is increased from 10−7 A/cm2 at 3 nm up to the range of 1 ~ 10−5 A/cm2 at 1.5 nm under 1 V in inversion regions [3], [4]. This excessive high current can conceivably alter a device’s performance, to say nothing of the difficulties associated with the large power dissipation. In addition, the boron impurity in pMOSFETs will penetrate from the p+-doped gate electrode into the oxide and underlying Si substrate [5]. Hence, to explore new materials for further gate dielectric application is urgent. Recently, high-K dielectrics, such as Ta2O5, TiO2, and BST have been studied as alternatives to silicon dioxide [6]. Unfortunately, most of these materials are not thermally stable on silicon and tend to form an interfacial SiOx film to reduce their effective capacitance. Furthermore, there are still the problems of integrating these materials into ever more complicated device processing.

Next, much attention has been paid to the ultrathin nitride to replace the conventional oxide. Indeed, nitride film exhibits several properties superior to silicon dioxide. The most important is that it can suppress the boron penetration and enhance the reliability. In addition, nitride film also exhibits about twice the dielectric constant of oxide. The higher dielectric constant of nitride allows a larger physical thickness to suppress the tunneling leakage current while maintaining the same gate capacitance. Furthermore, the excellent thermal stability of nitride makes it superior to high-K materials to be integrated into the CMOS process [7], [8]. However, poor nitride/Si interface results in poor performance of MOS device. Therefore, ultrathin nitride/oxide (N/O) stack has been investigated as a promising structure to solve this problem, because it has the advantage of nitride and still preserves the excellent oxide/Si interface.

Nevertheless, most of the proposed N/O stacks are still thicker than 1.9 nm, making them out of sorts for further ULSI applications. In addition, at the range of thickness, the replacement of oxide with N/O stack is not urgent. Since the leakage current of the 1.9 nm oxide is still much lower than the acceptable range of 1 A/cm2 under 1 V power supply for further deep submicrometer ULSI [3]. In this study, N/O stacks with thinner equivalent oxide thicknesses (EOTs) down to 1.6 nm prepared by rapid thermal chemical vapor deposition (RTCVD) with two-step NH3/N2O post-deposition annealing have been studied to meet the urgent requirement.

During the study, it was found that the types of the bottom oxide of the N/O stack dramatically influence the dielectric quality and device performances. In the past, much attention has been paid to electrical properties affected by the bottom oxide thickness and oxide/nitride EOT ratio [7]–[9] and very few studies have been about the different electrical behaviors of N/O stacks affected by different bottom oxide materials. In this study, bottom oxides grown in NO and in O2 ambient are compared. NO-grown bottom oxide, which is a nitrogen-rich oxide
layer, yields lower structure inconsistency with nitride than that of O$_2$-grown bottom oxide. In addition, this nitrogen-rich oxide layer can be like a diffusion barrier [10], to prevent nitrogen from being further driven into bottom oxide during the post-deposition NH$_3$ nitridation. The experiment results show that N/O stack with NO-grown bottom oxide exhibits lower flat-band voltage shift and superior hole and electron mobility, but inferior gate leakage current than that with O$_2$-grown bottom oxide in the same EOT.

Next, as most of the other deposition approaches, RTCVD process requires post-deposition annealing to stabilize the as-deposited films, drive hydrogen out, and minimize electrical defects [10]. However, the post-deposition treatment at any time will affect the film’s electrical thickness, dielectric quality, and the device performance. In the past, most investigations on post-deposition annealing effects were done in pure oxide or nitrided oxide and focused on the improvement of reliability only [10], [11]. In this paper, a two-step post-deposition treatment (NH$_3$ nitridation followed by N$_2$O annealing) has been proposed and optimized to examine the most important characteristics of gate dielectric, such as flat-band voltage shift, EOT variance, mobility deterioration, and leakage current reduction. The NH$_3$ nitridation step is applied to further reduce the EOT by increasing dielectric constant, while N$_2$O annealing is performed to improve the interface property and anneal out the defects caused by nitridation. The results show that increasing NH$_3$ nitridation temperature can make the N/O stack more stoichiometric, decrease EOT, and improve leakage current behavior, but the result is more severe mobility degradation. The N$_2$O annealing, on the other hand, can modify the interface property and improve the mobility, but it can cause the increase of EOT and worsen leakage current behavior, thus making a compensatory action to the NH$_3$ annealing.

II. EXPERIMENTAL

N- and p-channel MOSFET samples were fabricated on p-type Si(100) wafer using 0.15-$\mu$m dual-gate, twin-well CMOS technology. After trench isolation and active area definition, gate dielectrics were grown by RTCVD. The ultrathin oxide/nitride gate stacks were completed prior to exposure to the atmosphere. Standard RCA and in-situ ultraviolet (UV) Cl$_2$ vapor cleaning was performed to remove contaminant and native oxide for surface preparation. The bottom oxides with thickness of 0.8 nm were thermally grown in either NO or O$_2$ gas at 700 °C–850 °C, 100 torr. The split bottom oxides were used to investigate the bottom oxide effects on electrical properties. Next, high-quality chemical vapor deposited (CVD) nitrides with thickness of 1.4 nm were deposited at 750 °C, 1.5 torr, 25 s, using SiH$_4$ and NH$_3$ as source gases. After that, two-step post-deposition treatment, including NH$_3$ nitridation and subsequent N$_2$O annealing, were performed at different temperatures as following. First, NH$_3$ nitridation was done either at 850 °C or 900 °C, 500 torr, for 30 s to make the stack more stoichiometric. Then, the interfacial properties were modified by N$_2$O annealing either at 800 °C or 850 °C, 500 torr, for 30 s. In addition, the conventional oxides with different thickness were thermally grown to serve as samples for comparison. After the preparation of gate dielectrics, undoped polysilicon deposition, As/BF$_2$ implantation, patterning, and source/drain junction formation were performed. The source/drain activation annealing was done at 1075 °C by spike annealing. Then, cobalt silicide formation, Phosphosilicate glass (PSG) deposition, and contacts defining were executed on sequence. Finally, copper metallization was done to prepare samples for electrical characterization.

III. RESULTS AND DISCUSSIONS

A. Bottom Oxide Materials Effects

In general, a thin bottom oxide is always grown prior to the deposition of CVD silicon nitride film. Different types of bottom oxides exhibit different properties on these interfaces. Fig. 1 shows the flat-band voltage ($V_{FB}$) shifts of the N/O stacks with either O$_2$-grown or NO-grown bottom oxide as a function of growing temperatures. $V_{FB}$ shifts were defined as the changes of the $V_{FB}$ in comparison to that of the conventional oxide sample without diffusion barrier. All of these films were followed by the same nitride deposition and post-deposition annealing conditions. As shown in Fig. 1, $V_{FB}$ shifts of the N/O stacks with NO-grown bottom oxides are lower than that with O$_2$-grown bottom oxides. This is due to different structure inconsistency at the interface of the bottom oxide and Si$_3$N$_4$. It is well known that CVD nitride usually contains significant trapping at N/O interface and results in $V_{FB}$ shift in N/O stack [8], [12]. The bottom oxide grown in NO gas ambient is a nitrogen-rich oxide layer, which yields lower structure inconsistency than O$_2$-grown pure oxide does, when they come in contact with nitride films [10]. The lower structure inconsistency results in lower positive charges, thus lowering $V_{FB}$ shift. Furthermore, increasing growing temperature will get a higher degree of strain relief, which in turn reduces $V_{FB}$ shift in both O$_2$ and NO growing ambient [12], [13].

It is worthy to note that the flat-band voltage shifts in pMOSFETs are larger than those in nMOSFETs. The similar results have been observed in oxynitride prepared by remote plasma
We attribute the larger $V_{th}$ shift in pMOSFET to the following mechanisms. First, as proposed by Wang et al. [15], the magnitude of $V_{th}$ shift for ultrathin N/O gate stacks in MOS device depends on the Fermi level position in the gate material. There is a high density of donor-like interface states at the nitride/poly-Si gate interface. These interface states, which are near the valence band of the polysilicon, are filled (neutral) for $n^+$ poly and thus resulted in no additional $V_{th}$ shift. However, for $p^+$ poly, the donor-like states are empty, resulting in a net positive charge at the nitride-polysilicon interface. Second, Wu et al. [7] claimed that $V_{th}$ shift in pMOSFET comes from the boron penetration in the oxide device. Furthermore, 8 Å nitride film has been reported to effectively block the boron penetration [16], [17]. The nitride layer in N/O stack in this work has the thickness of 1.4 nm, which is reasonable to stop the penetration of boron. In order to distinguish these two mechanisms, the capacitance–voltage ($C–V$) curves of oxides with and without boron diffusion barrier have been measured and plotted in Fig. 2, in which N/O stacks with O$_2$-grown (700 °C) and NO-grown (800 °C) bottom oxides are also shown for comparison. Based on the anticipated value of $V_{th}$ as calculated from the poly-Si gate and substrate doping concentration, the $V_{th}$ shift of the control oxide without boron diffusion barrier indicates the boron penetration to the substrate [7]. Obviously, both mechanisms contribute to the larger $V_{th}$ shift in pMOSFETs. The donor-like states could be the additional positive charges in the N/O stacks, shifting the $C–V$ curve of the N/O stack toward the left, while the boron penetrated in the oxide shifts the $C–V$ curve of oxide to right, thus enlarging the $V_{th}$ shift in pMOSFETs.

The $C–V$ traces of the oxide/nitride stacks with either O$_2$-grown oxide or NO-grown oxide for nMOSFET in depletion regions are shown in Fig. 3. The EOT is extracted by $C–V$ simulator, which takes into account the quantum mechanical effects and poly-Si gate depletion effects [18]. The trace/retrace indicated by the arrows shows no hysteresis in $C–V$ curves for both kinds of N/O stacks. The negligible amounts of hysteresis in the N/O stacks are attributed to the elimination of bulk traps by the post-deposition annealing [19], which effectively reduces excess Si atoms and H-related species (such as Si-H bonds in the Si$_3$N$_4$ film), resulting in N/O stacks with more robust structure and less traps sites [20].

Fig. 4 demonstrates the gate leakage current density as a function of the gate voltage for pMOSFETs with different gate dielectrics. The inset shows TEM photos for (1) oxide and N/O stacks with either (2) O$_2$-grown or (3) NO-grown bottom oxide. The gate tunneling mechanisms of N/O stack are illustrated as follows. The gate current in inversion region is predominately due to the direct tunneling from the inversion layer to the gate electrode and the carrier supplied by source and drain. Hole tunneling from the valence band in the channel of the $p^+$ poly-Si PMOS dominates the gate leakage current [21]. When $0 > V_g > V_{th}$, both the $p^+$ polysilicon gate and the n-type substrate side are in depletion. Direct tunneling current between
the gate and channel is small, due to a few carriers available in the channel. However, in the source/drain extension (SDE) regions, holes in p+ polysilicon are in accumulation, leading to a dominated SDE-to-gate tunneling current. As $V_{gd} > V_{th}$, the substrate to the gate tunneling current increases quickly and becomes dominated [4], [22]. At the voltage range of $V_{gd} < 3$ V, the voltage across the N/O stack is less than 2 V. It is still less than the barrier heights of Si$_3$N$_4$ or SiO$_2$ (2.1 eV and 3.1 eV, respectively), thus the FN tunneling is neglected. Based on Figs. 4 and 5, one can observe that two kinds of N/O stacks exhibit substantially lower leakage currents than their oxide counterpart with the same EOT of 1.6 nm. This is due to the fact that N/O stack gate dielectric takes advantage of the higher dielectric constant of the nitride film, thus being permitted with a larger physical thickness for the same gate capacitance. In addition, the larger physical thickness offsets more than the barrier height lowering and gives rise to a lower tunneling probability [8]. Next, the N/O stack with O$_2$-grown oxide shows lower gate leakage current than that with NO-grown oxide of the same EOT as a result of thicker initial physical thickness of the N/O stack. The TEM photos of these three gate dielectrics are shown in the right inset of Fig. 4. The O$_2$-grown bottom oxide is thicker than the NO-grown one, in which the oxide growth rate may be retarded by the nitrogen. However, the EOTs of both types of bottom oxides are identical after the same nitride deposition and post-deposition annealing conditions. The results indicate that the post-deposition annealing will affect the two kinds of bottom oxides in the N/O stack differently. On the other hand, the lower gate leakage current of N/O stack also contributes to the transistor off-state current, as shown in the left inset of Fig. 4. It has been proven that the pMOSFET off-state current is dominated by the hole direct tunneling between SDE region to gate electrode [21], [22]. The N/O stack lowers the direct tunneling current between the SDE and the gate, thus reducing the off-state current. Therefore, the N/O stack with O$_2$-grown oxide obtains the lowest gate leakage current and results in the lowest off-state current.

Fig. 6 illustrates the effective mobility as a function of effective field for MOSFETs with different gate dielectrics. The effective mobility is extracted from $I_d$-$V_g$ curves in the linear region with $V_d = 0.1$ V. Large dimension transistors with $W/L = 10 \mu m/10 \mu m$ were used to avoid the short-channel effect, and the uncertainties from the source/drain series resistance. The two kinds of N/O stack show the deteriorated peak mobility in low field range and improved mobility in high field range, as compared to the oxide counterpart for nMOSFETs. However, the hole mobility is degraded at all field ranges for pMOSFETs with N/O stack gate dielectrics. The lowering of the peak mobility of N/O stacks are attributed to an increase in the scattering rate due to the presence of the nitrogen, which enhances Coulombic and filled electron trap scattering [23]. The opposite mobility behaviors for nMOSFET and pMOSFET in high field regions are due to the incorporation of nitrogen in the interface to reduce the acceptor-type states above the conduction band and the increase in the donor-type states below the valence band, resulting in an improvement of electron high field mobility and a degradation of hole high field mobility [23], [24]. Based on the above discussions, the N/O stack with NO-grown bottom oxide exhibits a small amount of flat-band voltage shift (<20 mV), which means only a small amount of nitrogen is incorporated near the interface. In addition, the degradation in peak mobility is only 4% as compared to its 1.6-nm oxide counterpart. The degradation is still acceptable in device scaling for ULSI application [25]. However, the N/O stack with O$_2$-grown bottom oxide suffers from larger flat-band voltage shift and large amounts of nitrogen incorporation.

B. Two-Step Post-Deposition Annealing Effects

1) NH$_3$ Annealing: As discussed previously, the N/O stack with NO-grown bottom oxide is more suitable for deep submicrometer dual-gate CMOS application, but suffers from the
worse gate leakage current reduction, which can be recovered by following NH \textsubscript{3} anneal for getting a more stoichiometric nitride film. As listed in Table I, decreasing the EOT of the stacks is observed with the increase of the NH \textsubscript{3} nitridation temperature. This is due to more nitrogen incorporation with higher nitridation temperature, thus enhancing the dielectric constant and reducing the EOT. Furthermore, the flat-band voltage of N/O stacks are all shifted to the left (i.e., with a negative value of flat-band shift) after the NH \textsubscript{3} annealing, thus indicating the generating positive charge traps in the gate stacks as well as at the interfaces [15].

Although higher NH \textsubscript{3} anneal temperatures can further stabilize the film structure and reduce the EOT, this also results in an undesirable degradation in transistor’s mobility in N/O stack, as shown in Fig. 7. The effective mobility deteriorated as nitridation temperature increased from 850 °C to 900 °C. This is attributed to the presence of nitrogen, which enhances the Coulombic and the filled electron trap scattering [23], [24].

The leakage current reduction rate is always used as a good merit to investigate the leakage current behavior of N/O stacks in comparison with the oxide of identical EOTs. The leakage current reduction rate $R$ is defined as the ratio of leakage current in oxide device to that in N/O stack device with identical EOTs, i.e., $R = J_{G, \text{oxide}} / J_{G, \text{N/O stack}}$ at $V_{G} - V_{\text{th,oxide}} = -1$ V. The gate leakage is compared at a normalized voltage ($V_{G} - V_{\text{th,oxide}} = -1$ V); thus, the unfair comparison caused by the differences in flat-band voltage (and thus threshold voltage) among the various gate dielectric recipes can be eliminated. Fig. 8 shows the gate leakage current densities versus EOT for both oxide gate and N/O stacks with different NH \textsubscript{3} annealing temperatures. Based on the measured leakage current densities, different $R$ values were calculated and shown in the figure.

The gate leakage currents in oxide gate dielectrics are very consistent with the previously reported data [4], [5]. All stacks yield much lower gate leakage currents than their oxide counterparts with the same thicknesses. This shows that increasing NH \textsubscript{3} nitridation temperature just slightly increases the leakage current. Since the stacks preserve the same physical thicknesses, as shown in the inset of Fig. 8, the slight increase in leakage current with increasing NH \textsubscript{3} nitridation temperature could be ascribed to the lowering of barrier height in stack by increasing nitride incorporation [6]. A more obvious advantage to increasing NH \textsubscript{3} nitridation temperature is the improvement of the leakage current reduction rate. The value of $R$ is improved from 5.6 to 7.5 for the reduction of EOT in a higher NH \textsubscript{3} nitridation temperature.

2) Subsequent N\textsubscript{2}O Annealing: Although the first NH \textsubscript{3} annealing step enhances the nitride films with more stoichiometric and improves the gate leakage current reduction, the annealing of NH \textsubscript{3} also introduces high concentrations of hydrogen into dielectric which act as traps, and need to be removed in a hydrogen-free ambient [10]. Hence, the N\textsubscript{2}O annealing is added subsequently to the NH \textsubscript{3} annealing. As listed in Table I, increasing N\textsubscript{2}O anneal temperature will increase the final thickness owing to the additional oxide growth at the Si/SiO\textsubscript{2} interface. This anneal-induced reoxidation modifies the Si/SiO\textsubscript{2} interface as well as decreases the flat-band voltage shift [7], [11]. In addition, the reoxidation of the Si/SiO\textsubscript{2} interface removes

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**Table I**

<table>
<thead>
<tr>
<th>Annealing Type</th>
<th>Annealing Temperature</th>
<th>EOT (Å)</th>
<th>$V_{fb}$-shift (mV)</th>
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<td>N\textsubscript{2}O isothermal</td>
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<td></td>
<td>N\textsubscript{2}O 800°C</td>
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<td></td>
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<tr>
<td></td>
<td>NH\textsubscript{3} 900°C</td>
<td>15.5</td>
<td>-233</td>
</tr>
<tr>
<td></td>
<td>N\textsubscript{2}O 800°C</td>
<td></td>
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<tr>
<td>NH\textsubscript{3} isothermal</td>
<td>NH\textsubscript{3} 900°C</td>
<td>15.5</td>
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<tr>
<td></td>
<td>N\textsubscript{2}O 850°C</td>
<td>18.7</td>
<td>-205</td>
</tr>
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</table>

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**Fig. 7.** Effective mobility as a function of effective field at different NH\textsubscript{3}/N\textsubscript{2}O annealing conditions.

**Fig. 8.** Gate leakage current as a function of EOT at different NH\textsubscript{3}/N\textsubscript{2}O annealing conditions. The inset shows the TEM photos of N/O stacks with different annealing conditions.
the nitrogen from interface [7], [9], thus improving the mobility, as shown in Fig. 7. The effective mobility is increased by increasing the N2O annealing temperature from 800 °C to 850 °C.

Raising the N2O annealing temperature, however, will regrow the bottom oxide at the same time, as examined by the TEM photos shown in the inset of Fig. 8, where the bottom oxide thickness increases from 21 Å to 25 Å with the N2O annealing temperature increasing from 800 °C to 850 °C. The regrowth of bottom oxide then reduces the N/O ratio in the N/O stack, which affects the gate tunneling leakage current in N/O stacks, as reported previously [8]. Thus, the value of R is decreased from 7.5 to 6.1 with the N2O annealing temperature raising from 800 °C to 850 °C. Therefore, a tradeoff between leakage current reduction and transconductance shall be done in setting the temperatures of the post deposition treatment.

IV. CONCLUSION

Ultrathin N/O gate stacks with EOT of 1.6 nm, prepared by RTCVD and two-step NH3/N2O post-deposition treatment, for dual-gate CMOS have been studied experimentally. In addition, the electrical properties of the N/O stacks were optimized with bottom oxide materials and the post-deposition treatment. The ultrathin N/O stack with NO-grown bottom oxide exhibits fewer flat-band voltage shift (<20 mV), higher hole and electron mobility, and is good enough for near future deepsubmicrometer CMOS application. However, the N/O stack with NO-growth bottom oxide suffers a worse leakage current reduction than that with O2-grown bottom oxide. Fortunately, a two-step post annealing, which consists of the NH3 nitridation and the subsequent N2O annealing, can compensate the deteriorated leakage current reduction in N/O stacks with NO growth bottom oxide.

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REFERENCES

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