Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metal–oxide–semiconductor field-effect transistors for high-k-HfO₂ dielectric

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Hafnium dioxide (HfO₂) gate dielectrics formed by the atomic layer deposition (ALD) process were fabricated to investigate the flatband voltage shift (∆V_{FB}) relative to SiO₂. It is found that the direction of ∆V_{FB} depends on the Fermi level position in the gate material, which shows respective positive and negative shifts in n-type and p-type metal–oxide–semiconductor field-effect transistors (MOSFETs), regardless of the substrate type. The opposite direction in the flatband voltage shift is attributed to both acceptor- and donor-like interface states existing at the interface between the polycrystalline-silicon (poly-Si) gate and HfO₂ dielectric. A model is proposed to explain the effects of poly-Si gate type on the flatband voltage shift in MOSFETs. © 2003 American Institute of Physics. [DOI: 10.1063/1.1592634]

The exponential increase in the gate leakage current with decreasing oxide thickness poses a major limitation for the usefulness of conventional SiO₂. In order to reduce the gate tunneling current while simultaneously maintaining the same gate capacitance, high-k gate dielectrics become one of the solutions for advanced complementary metal–oxide–semiconductor (CMOS) applications.

Among the high-k dielectrics, hafnium dioxide (HfO₂) appears promising due to its relatively high dielectric constant (~25), wide band gap (~5.8 eV), and calculated thermodynamically stability in contact with Si. Moreover, the integration of HfO₂ into sub-100 nm device has been reported recently. However, device parameter issues such as memory window, mobility, and threshold voltage shift remain unsolved. This is important because a high threshold voltage shift will prevent a device from working within the criteria for the sub-100 nm technology node. Therefore, the cause of the flatband voltage (V_{FB}) shift for HfO₂ high-k dielectrics must be understood.

Previous studies using nitride gate dielectrics found that the V_{FB} has a tendency to shift negatively due to the fixed positive charge and that this phenomenon is enhanced in p-type metal–oxide–semiconductor field-effect transistors (pMOSFETs). On the contrary, studies on Al₂O₃ gate dielectrics found a positive V_{FB} shift, which can be explained by the creation of fixed negative charges, and is enhanced in n-type MOSFETs (nMOSFETs). In this work, HfO₂ was found to exhibit a positive ∆V_{FB} for nMOSFETs and a negative ∆V_{FB} for pMOSFETs, respectively. The origin of this polycrystalline-silicon (poly-Si) gate type dependency is attributed to both donor- and acceptor-like interface states at the poly-Si and HfO₂ interface.

pMOSFETs with a P+ type gate and nMOSFETs with a n+ type gate were fabricated using a dual gate CMOS twin-well technology. After trench isolation and active area definition, standard SC1/SC2 clean processes were performed on all wafers. The SC1/SC2 clean not only removes the native oxide fully, but also grows about a 8 Å chemi-cal oxide, which serves as a good interfacial layer between HfO₂ and silicon substrate. Then, a 4-nm-thick HfO₂ film was deposited by atomic layer deposition at substrate temperature of 300 °C using HfCl₄ and H₂O as precursors. A conventional oxide of 1.8 nm was grown for comparison. Next, a 150-nm-thick undoped poly-Si film was deposited and patterned. The n+ poly-Si gate was doped with a 25 keV 1×10¹⁵ cm⁻² implant dose of phosphorus and the p+ poly-Si gate was doped with a 10 keV 3.5×10¹⁵ cm⁻² implant dose of boron. Then a spike activation anneal was done at 1050 °C. Subsequent processing steps follow a typical self-aligned MOSFET process flow. A series of HfO₂ capacitors with n+ and p+ poly-Si gates on both n-well and p-well substrates were also fabricated. The equivalent oxide thickness (EOT) extraction and V_{FB} values were extracted using a capacitance–voltage (C–V) simulator, which takes into account poly-Si depletion and quantum mechanical effects.

Figure 1 illustrates the C–V curves for nMOSFET devices with SiO₂ and HfO₂ gate dielectrics. Clearly, the V_{FB} of the HfO₂ is shifted positively compared to the SiO₂. The EOT of both gate dielectrics are similar at approximately 18 Å. Figure 2 shows the C–V curves for pMOSFET devices. In contrast, the V_{FB} of HfO₂ shifts negatively with respect to SiO₂. The bidirectional shift is interesting. Factors leading to the V_{FB} shift are fixed charges, interface traps, and dopant diffusion. However, fixed charges only cause unidirectional V_{FB} shift, since the polarity of fixed charge is unique, i.e., positive or negative. Although Lee et al. reported that phosphorus diffuses into Al₂O₃ can cause V_{FB} shift, but the shift
is unidirectional. Next, Onishi et al. have found phosphorus or boron penetration into HfO$_2$ also induces bidirectional $V_{FB}$ shift. Nevertheless, the shift directions are negative and positive with respective to the SiO$_2$ for phosphorus penetration in $n$-MOS and for boron penetration in $p$-MOS, respectively. That is, the opposite direction to our observation. Hence, we suggest the bidirectional shift in this work is not due to dopant diffusion but attribute to interface traps, which exist at both HfO$_2$/Si and poly-Si/HfO$_2$ interfaces.

To clarify the origins contributing to the opposite $V_{FB}$ shift, a series of HfO$_2$ and SiO$_2$ capacitors with $n+$ and $p+$ poly-Si gates, each on both $p$- and $n$-well substrates were fabricated. Table I summarizes the $V_{FB}$ of the four structures: $n+$ poly-Si/$p$-substrate, $n+$ poly-Si/$n$-substrate, and $p+$ poly-Si/$p$-substrate for both HfO$_2$ and SiO$_2$ dielectrics. The $V_{FB}$ shift was calculated by subtracting the $V_{FB}$(SiO$_2$) from the $V_{FB}$(HfO$_2$). Based on Table I, all capacitors with $n+$ gates show positive $\Delta V_{FB}$ of 300 mV, regardless of the substrate type. On the contrary, all capacitors with $p+$ gates show negative $\Delta V_{FB}$ of 400 mV. Therefore, the direction of $V_{FB}$ shift for HfO$_2$ films in MOS devices is predominated by the poly-Si/HfO$_2$ interface. Additionally, the magnitude of $\Delta V_{FB}$ is slightly higher in $p$-MOS than in $n$-MOS devices.

<table>
<thead>
<tr>
<th>Case</th>
<th>Gate</th>
<th>Sub.</th>
<th>$V_{FB}$(HfO$_2$) (V)</th>
<th>$V_{FB}$(SiO$_2$) (V)</th>
<th>$V_{FB}$ Shift (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N+</td>
<td>P</td>
<td>-0.769</td>
<td>-1.07</td>
<td>301</td>
</tr>
<tr>
<td>2</td>
<td>N+</td>
<td>N</td>
<td>0.177</td>
<td>-0.117</td>
<td>294</td>
</tr>
<tr>
<td>3</td>
<td>P+</td>
<td>N</td>
<td>0.524</td>
<td>0.927</td>
<td>-403</td>
</tr>
<tr>
<td>4</td>
<td>P+</td>
<td>P</td>
<td>-0.488</td>
<td>-0.034</td>
<td>-454</td>
</tr>
</tbody>
</table>

**FIG. 1.** $C$–$V$ curves of $n$MOSFET devices with HfO$_2$ and SiO$_2$ dielectrics. The area is 1000 $\mu$m$^2$. The EOT is maintained at approximately 1.8 nm for both dielectrics.

**FIG. 2.** $C$–$V$ curves of $p$MOSFET devices with HfO$_2$ and SiO$_2$ dielectrics. The area is 1000 $\mu$m$^2$. The EOT is maintained at approximately 1.8 nm for both dielectrics.

**FIG. 3.** Schematic band diagrams considering both acceptor- and donor-like interface states locating at polycrystalline-silicon gate and HfO$_2$ interface. An acceptor-like interface state is neutral or negative by accepting an electron, with its largest density populating near the conduction band edge. A donor-like interface state is neutral or positive by donating an electron, with its largest density populating near the valence band edge.
To explain the bidirectional $V_{\text{FB}}$ shift, we propose the model in Fig. 3, which takes into account both donor- and acceptor-like interface states at poly-Si and dielectric interface. An acceptor-like interface state is neutral or negative by accepting an electron, with its largest density populating near the conduction band edge. A donor-like interface state is neutral or positive by donating an electron, with its largest density populating near the valence band edge. When the poly-Si gate is $n$ type, the Fermi level is located at the bottom of conduction band. The interface states with its energy level below Fermi level are filled. Therefore, the donor-like interface states are electrically neutral and acceptor-like interface states are electrically negative, resulting in net negative charges. On the other hand, when the poly-Si is $p$ type, the Fermi level is located near the top of valence band. Therefore, most of the acceptor-like interface states are empty and electrically neutral. However, parts of the donor-like interface states are unfilled and electrically positive, resulting in net positive charges and contributing to the negative $V_{\text{FB}}$ shift in $p$-MOSFETs.

As to the larger magnitude of $V_{\text{FB}}$ shift in $p$-MOSs than in $n$-MOSs, it is probably because the depletion layer of the $p$-type poly-Si is more severe than the $n$-type poly-Si, due to the inherent nature of implanted species.

In summary, the flatband voltage shift for HfO$_2$ films in $n$-MOSFETs and $p$-MOSFETs is caused by the Fermi level in the gate material, and is independent of the substrate type. A model based on the surface states at the interface of poly-Si and HfO$_2$ is proposed. For $n$-type poly-Si, acceptor-like interface states are electrically active and lead to positive flat-band voltage shift. Donor-like interface states are electrically active in $p$-type poly-Si gates, resulting in negative flatband voltage shift. Furthermore, the magnitude of flatband voltage shift is slightly larger for $p$-MOSFETs than for $n$-MOSFETs and is probably due to a high poly-Si depletion for the $p$-type poly-Si.

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