RRAM SET Speed-Disturb Dilemma and Rapid Statistical Prediction Methodology

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Abstract

This paper presents a first comprehensive study of SET speed-disturb dilemma in RRAM using statistically-based prediction methodologies. A rapid ramped-voltage stress based on percolation model and power-law \( V-t \) dependence showed excellent agreement with the time-consuming constant-voltage stress, and was applied to evaluate current status of RRAM devices in the literature.

Introduction

Resistive-switching random access memory (RRAM) has the potential to become the front runner for future nonvolatile memory. SET/RESET in RRAM has been explained by partial connection and rupture of conducting filaments (CFs) in metal oxides [1]. Furthermore, the disturb of high resistance state (HRS) is analogous to SET except occurred at a lower disturb voltage \( (V_{\text{DIS}}) \) rather than a higher SET voltage \( (V_{\text{SET}}) \). \( V_{\text{DIS}} \) may be the read voltage or in a crossbar RRAM at least \( V_{\text{SET}}/3 \) on the write disturb bits using a V3 scheme [2]. Theoretically desired SET speed \( (t_{\text{SET}} < 1 \mu s) \) and disturb immunity \( (t_{\text{DIS}} > 1 s \text{ or } 10^6 \text{ cycles}) \) may be designed using the highly nonlinear voltage-time \( (V-t) \) dependence at SET [3-6]. However, whether or not there exists an acceptable design space remains to be explored. Further complexity arises from the challenge of significant cycling variation at SET. This intrinsic stochastic nature of reconnecting ruptured CFs was explained by the percolation model [7], widely adopted in dielectric breakdown. However, many studies on SET speed and read/write disturb had reported only the results from a single measurement. Statistically significant data taking into account variation has not received enough attention, despite being technologically important for high-density memory applications.

This paper presents a first comprehensive study of the SET speed-disturb dilemma using a statistically-based prediction methodology. The validation of the percolation model was first performed on the SET variation of two distinct RRAM devices, Ti/TiO\(_2\)/Pt based on valance-change mechanism [8] and Ni/HfO\(_2\)/Si based on both electrochemical and thermochemical mechanism [9]. The power-law \( V-t \) dependence was verified across ten orders of magnitude in time using constant voltage stress (CVS). Additionally, a rapid prediction method based on ramped voltage stress (RVS) showed excellent agreement with the CVS data, but took only a fraction of time. It also agreed with the numerical RRAM simulation based on the percolation model. Finally, taking advantage of the rich RVS data available in the literature, the current status of RRAM devices to meet the strict requirement of the SET speed-disturb dilemma is discussed.

RRAM Percolation and Voltage Acceleration Model

Figure 1 displays typical bipolar resistive switching (RS) in the TiO\(_2\) and HfO\(_2\) RRAM. Figure 2 shows that the SET variation in an identical cell under cycling was much larger than that between different cells. Therefore, it is regarded as the fundamental limit in high-density memory array and the main focus of this study. \( t_{\text{SET}} \) was measured at constant voltages using a DC setup in Fig. 3 and a pulse setup in Fig. 4 for different \( t_{\text{SET}} \) ranges. The identical cell was cycled by bipolar RESET after every SET. Figure 5 shows that \( t_{\text{SET}} \) of the TiO\(_2\) device using both setups followed a classical Weibull distribution defined by \( t_{\text{SET}} \) at the 63rd failure percentile \( t_{63\%} \) and the Weibull slope \( \beta \), as predicted in the percolation model. The constant \( \beta \) across eight orders of magnitude in \( t_{\text{SET}} \) revealed a monomodal distribution independent of the measurement setups. \( \beta \) in both the TiO\(_2\) (0.3 in Fig. 6) and HfO\(_2\) (0.37 in Fig. 7) devices showed little dependence on the CVS voltage \( (V_{\text{CVS}}) \), in good agreement with the percolation model. The demonstration of a constant \( \beta \) related to SET variation allows accurate yield prediction in high-density arrays by statistical extrapolation. Figure 8 shows the highly nonlinear power-law \( V-t \) relation across ten orders of magnitude in \( t_{\text{SET}} \). The power-law dependence has been widely adopted in the ultra-thin oxide breakdown theory [10], and is consistent with the partial connection of ruptured CFs. The various \( V-t \) relations reported in different RRAMs [3-5] may also be fit using different acceleration exponent \( n \) with good accuracy. Once the \( n, t_{63\%}, \) and \( \beta \) are known, Fig. 9 illustrates the extrapolation procedures to the use conditions with desired SET and disturb failure rate (FR) of 1 ppm.

Rapid RVS Prediction Methodology

The RVS method is equivalent to a series of discrete CVS with linearly ascending stress voltages, which is typically several orders of magnitude faster than the conventional CVS in studying cycling variation and voltage acceleration. Figure 10 shows that the measured SET voltage by RVS \( (V_{\text{SET,RVS}}) \) complied with the Weibull distribution, in excellent agreement with our RRAM simulation using a percolation-based model [11]. The CVS parameters, \( n, t_{63\%}, \) and \( \beta \), may be extracted from the RVS parameters, ramped rate (RR), \( V_{63\%}, \) and \( \beta_{\text{RVS}}, \) using the formulas in Table 1 [6,12-13],

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both methods in Fig. 8 and 11, and the excellent agreement was validated by the nearly identical \( \beta \) distributions were used to extract using the power-law voltage criterion for crossbar RRAMs (\( V \)) shows the complete flow to extract the dependence of a desired SET/read disturb voltage criterion (\( V \)) was also attempted in Fig. 19. In addition to the prediction power, the RVS methodology may be applied to gauge the current status of SET speed-disturb dilemma using devices reported in the literature. In contrast to the lack of statistical data for SET speed or disturb, cycling variation in RRAM devices is often tested by DC voltage sweep, which is directly related to the RVS method. The reported statistical \( \beta \) distributions were used to extract \( \beta \) and \( \beta \) and predict \( \beta \) and \( \beta \) with the exception of a CuO device that might meet the SET/read disturb voltage criterion. Immunity to write disturb in crossbar RRAMs is even more difficult to satisfy, unless \( \beta \) is greatly relaxed. Future RRAM research on improved \( \beta \) and \( \beta \) is required to address the design constraint of the SET speed-disturb dilemma.

**Conclusion**

A comprehensive study on the SET speed-disturb dilemma using a statistically-based prediction methodologies has been reported. Based on the percolation model and power-law \( V-t \) dependence, a rapid RVS method was proposed to reduce the analysis time and cost as compared with the conventional CVS method. Additionally, this study provided a useful design guideline to optimize the SET speed-disturb performance in RRAM using easily accessed DC cycling data. The survey of the current RRAM devices reported in the literature confirmed that the SET speed-disturb dilemma would probably continue to pose challenges in implementing high-density RRAM arrays in the future.

**Acknowledgments**

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**References**


RS characteristics of HfO$_2$ and TiO$_2$ devices. RS in HfO$_2$ was more abrupt with larger HRS resistance than that in TiO$_2$ because of their different RS mechanism.

**Fig. 1**  
RS characteristics of HfO$_2$ and TiO$_2$ devices. RS in HfO$_2$ was more abrupt with larger HRS resistance than that in TiO$_2$ because of their different RS mechanism.

**Fig. 2**  
$V_{\text{SET}}$ distribution of six devices at different sites in a wafer. The solid black line represents the collected distribution of all devices. Cycling variation was much larger than that among different devices.

**Fig. 3**  
Schematic of DC CVS setup used for $t_{\text{SET}}$ ranging from 20 ms to 1000 s and a typical current–time trace. Current compliance was set the same as that in RVS.

**Fig. 4**  
Schematic of pulse CVS setup used for $t_{\text{SET}}$ ranging from 100 ns to 40 ms and a typical voltage–time trace. $R_{\text{load}}$ was used as a current limiting resistor.

**Fig. 5**  
Weibull distribution of the TiO$_2$ device measured at 0.75 V CVS using both the DC and pulse setups. A constant $\beta$ was independent of measurement setups.

**Fig. 6**  
Weibull distribution of the TiO$_2$ device measured at different CVS voltages, showing a constant $\beta$ of 0.3.

**Fig. 7**  
Weibull distribution of the HfO$_2$ device measured at different CVS voltages, showing a constant $\beta$ of 0.37.

**Fig. 8**  
Power-law $V$–$t$ relation obtained in this work. Reported data of other RRAMs in the literature [3-5] are also plotted.

**Fig. 9**  
Prediction of disturb time ($F=1$ ppm) and set time ($F=99.9999 \%$) at 1 ppm failure rate.

**Table 1**  
Derivation of the RVS-CVS conversion formulas.
Table 2 | V₆₃% and βₓRVS extracted from VSET distribution of various RRAM devices in the literature. If not stated in the literature, RR was assumed to be 0.1 V/s to 10 V/s, which are typical values in semiconductor parameter analyzers such as Agilent 4156. The n factor was assumed to be 20 to 50 according to Fig. 8.

<table>
<thead>
<tr>
<th>Material</th>
<th>Vₓ₆₃%</th>
<th>βₓRVS</th>
<th>Reference</th>
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<tr>
<td>a</td>
<td>CsCuO₀·CuPt</td>
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<td>15.41</td>
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<td>b</td>
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<td>Ru/Ta/On/TiO₂/Ru</td>
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<td>8.06</td>
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<tr>
<td>f</td>
<td>Ti/Ta/On/Ti/N</td>
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<td>8.56</td>
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<tr>
<td>h</td>
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<tr>
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<tr>
<td>j</td>
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<tr>
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<tr>
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<tr>
<td>m</td>
<td>Ni/Co/On/Th</td>
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Fig. 11 (left) VSET_RVS distributions obtained using different ramp rates. (right) F₆₃% versus RR in a double-logarithmic plot, where the slope corresponds to n + 1.

Fig. 12 Iₖ₆₃% measured by CVS (square symbols) and converted from RVS (solid lines) at different VCVS.

Fig. 13 Flow chart of VSET and VDIS prediction at 1 ppm FR using RVS.

Fig. 14 Projection of desirable VDIS for 1 s tₖ₆₃% and VSET for 1 µs tₖ₆₃% at 1 ppm FR. Symbols refer to the measured tₖ₆₃% by multiple CVS, and lines refer to the tₖ₆₃% converted from RVS.

Fig. 15 (left) Schematic plot of VSET_RVS distributions with different βₓRVS. (right) Predicted F₆₃% and VSET versus βₓRVS with a fixed V₆₃% and n.

Fig. 16 (left) Schematic plot of VCVS-6₃% relation with different n. (right) Predicted VDIS and VSET versus n with a fixed V₆₃% and βₓRVS.

Fig. 17 Predicted VDIS and VSET Versus F₆₃%, and βₓRVS with a fixed n of 20. Projected shadow regions represent the available design space for VDIS>0.5 V and VSET<3 V (FR < 1 ppm, tSET < 1 µs, tDIS > 1 s).

Fig. 18 Projected shadow regions extracted from Fig. 17. The intersection region represents available design space for a desired SET/read disturb voltage criterion.

Fig. 19 Prediction of RVS parameters n, F₆₃%, and βₓRVS necessary for a desired SET/read disturb voltage criterion (bottom) and SET/write disturb voltage criterion (up). Both tₖ₆₃%=1 s and a relaxed tₖ₆₃%=1 ms are shown.