3D Vertical TaOₓ/TiO₂ RRAM with over 10³ Self-Rectifying Ratio and Sub-μA Operating Current

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Abstract

The 3D double-layer vertical RRAM with ultralow sub-μA operating current and high self-rectifying ratio over 10³ has been demonstrated for the first time. This Ta/TaOₓ/TiO₂/Ti interfacial switching device overcomes the intrinsic trade-off between operating current and variability in filamentary RRAMs and shows promising potential for high-density data storage.

Introduction

Although 3D NAND technology promises to increase bit density beyond the conventional 2D memory [1], the fundamental limits of charge-based NVM such as the dwindling amount of stored electron and difficult transistor scaling remain daunting challenges [2]. Thus, vertical RRAM (Fig. 1) with better memory performance, ease of fabrication, and removal of vertical transistors inside the core array is under active development as an ultimate 3D NVM memory. The previous demonstrations of vertical RRAM, however, were either lack of sufficient nonlinearity to suppress parasitic sneak current in high-density arrays [3-4] or incompatible to semiconductor fabrication by using noble metal electrodes such as Pt [5]. Additionally, the operating currents were all above 50 μA, which exceeds the driving capability of the peripheral nanoscale transistor. Recently, we have successfully fabricated a bipolar Ta/TaOₓ/TiO₂/Ti RRAM with numerous highly desired features, including: extremely high endurance, forming free, self-compliance, self-rectification, multiple-level-per-cell capability, room-temperature process, and fab-friendly materials [6]. In this paper, we further demonstrate the first 3D vertical RRAM meeting the requirements of over 10³ self-rectifying ratio and sub-μA operating current by using the Ta/TaOₓ/TiO₂/Ti cell. Comprehensive circuit analysis shows that high-density 10-Mb arrays can be realized by considering read/write margins and transistor driving capability.

Device Fabrication

Fig. 2 shows the detailed process flow of 3D double-layer vertical RRAM fabrication. Multiple Ti (100 nm)/SiO₂ (100 nm) layers were deposited by PVD and PECVD, respectively. Patterning and dry etching were applied to form a vertical pillar structure with varied sidewall lengths. 40-nm TiO₂ and 20-nm TaOₓ were deposited sequentially on the pillar sidewall by PVD. Note that other conformal deposition techniques such as ALD with thinner film thicknesses would benefit the pitch-size scaling of 3D arrays in the future. The contacts to the Ti horizontal electrodes of the top and bottom cells were exposed by using two additional masks and dry etching. Finally, the Ta vertical electrode was deposited by PVD and patterned by a lift-off process. Fig. 3 shows the TEM image of the double-layer vertical RRAM. In contrast to the tapered sidewall using the Pt bottom electrode [5], using the fab-friendly Ti horizontal electrode formed a very steep sidewall profile, critical for future high-density integration. Fig. 4 shows the corresponding EDX profiling.

Device Performance

Fig. 5 shows extremely stable bipolar resistive switching (BRS) characteristics at both top and bottom cells. The devices required no electrical forming and current compliance, which greatly reduce the complexity of peripheral circuit design. The effective device area at the vertical sidewall was 0.2 μm². Most device characteristics resembled those previously reported in the planar device with a much large area [6]. The 10x resistance change at HRS/LRS can only be readout at negative bias. The rectifying ratio (RR) at ±2 V exceeded three orders of magnitude. However, in this vertical RRAM with scaled areas the maximum reset current can be further reduced to sub-μA, essential for implementing high-density arrays. Figs. 6 and 7 show the extremely tight distributions of R_HRS, R_LRS, and RR at both the top and bottom cells. Excessive switching variability is known to be the major bottleneck of RRAM. It was reported that the variability became even more severe in the sub-μA filamentary RRAM [7]. Our new results are encouraging for developing low-power RRAM with minimal variability. Furthermore, Figs. 8 and 9 show no retention degradation over 10⁴ s and read disturb immunity over 10⁵ cycles, respectively. Z (vertical) disturb through the vertical capacitive coupling is reported to be the major program disturb mechanism in vertical memory arrays [8]. Fig. 10 shows that the state of the bottom cell was not disturbed by the BRS at the top cell. Figs. 11 and 12 show the excellent pulse endurance over 10¹⁰ cycles using a 1-μs write pulse. The longer pulse width as compared with that in [6] was attributed...
to the unoptimized RC delay in our vertical RRAM structure.

Switching Mechanism

The proposed device is significantly different from the conventional filamentary RRAM in many aspects of device characteristics, such as forming free, self-compliance, self-rectifying, and highly stable BRS. The device currents at HRS/LRS both showed an apparent area dependence (Fig. 13), supporting an interfacial rather than filamentary switching mechanism [9-10]. BRS was believed to be originated from the modulation of Schottky barrier at the Ta/TaOx interface by the oxygen-vacancy (V_o) concentration (Fig. 14) [6]. The discontinuity of conduction bands at the TaOx/TiO2 interface suppressed electron injection from the Ti electrode at positive bias and thus enhanced IV asymmetry. Homogeneous interfacial switching overcome the intrinsic trade-off between operating current and variability in filamentary RRAMs, where the tradeoff was attributed to the very few V_o involved in BRS [7].

High-Density Array Analysis

An all-line pull-up scheme (Fig. 15) was used at read to provide high read throughput [11]. A sufficient read margin (Fig. 16) and a maximum read current below 10 μA (Fig. 17) can be realized in a 10-Mb array. Two write schemes, i.e. the conventional symmetric 1/3 scheme [12] and a novel asymmetric 3/4 set - 1/4 reset scheme (Fig. 15), were compared. Both require the same three voltage levels. Because of the large cell resistance, the interconnect resistance had negligible effects on the voltage delivery for the array size of the interests regardless of the write schemes (Fig. 18). Therefore, sufficient write margin can be designed easily in large arrays. The write current compatible to the transistor driving capability remained the major concern for implementing high-density arrays. Because of the asymmetric device IV, the reset sneak current through the half-selected bits biased at V_{RESET}/3 was the main bottleneck by using symmetric write schemes. By contrast, the asymmetric scheme reduced the bias on the half-selected bits to V_{RESET}/4 and the maximum set/reset current was kept below 10 μA in the 10-Mb array (Fig. 19). Fig. 20 shows the worse-case write disturb immunity over 10^12 cycles at the half-selected bits biased at 3/4 V_{SET}.

Conclusion

The 3D vertical RRAM with sufficient nonlinearity to suppress parasitic sneak current has been demonstrated by using interfacial switching in a fab-friendly Ta/TaOx/TiO2/Ti cell. Furthermore, the ultralow sub-μA operating current may be realized with minimal cycling variation, in contrast to the intrinsic trade-off in filamentary RRAMs. The numerical array analysis shows the promising potential of the proposed device for high-density data storage.

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References


Fig. 1 Schematic diagram of 3D vertical RRAM array for realizing high bit-density NVM.

Fig. 2 (a)-(e) Process flow of 3D double-layer vertical RRAM fabricated at room temperature using only four masks. (f) Cross-sectional view along the A-B cutline, showing the top and bottom unit cells at the vertical sidewall.

Fig. 3 (a) Cross-sectional TEM image of the 3D double-layer Ta/TaOx/TiO2/Ti vertical RRAM, showing a very steep sidewall profile. (b) and (c) show the enlarged pictures of the top and bottom cells. TaOx and interfacial TiOx were amorphous while TiO2 was polycrystalline.

Fig. 4 EDX analysis of the Ta/TaOx/TiO2/Ti stack at the vertical sidewall. The TaOx and interfacial TiOx layers appeared to be oxygen deficient.

Fig. 5 BRS characteristics using $V_{SET}$ of 5 V and $V_{RESET}$ of -6 V at both top and bottom cells. The effective device area at the vertical sidewall was 0.2 $\mu$m$^2$.

Fig. 6 Cumulative $R_{HRS}$ and $R_{LRS}$ distributions at both top and bottom cells. Stable 10x resistance change was read at -2 V.

Fig. 7 Cumulative current rectifying ratio (RR) distributions at both top and bottom cells. Rectifying ratio (RR) of $10^3$ is defined at ±2 V.

Fig. 8 Retention time over $10^7$ s at both top and bottom cells.

Fig. 9 Read disturb immunity over $10^6$ cycles at both top and bottom cells using a -2 V read pulse for 1 $\mu$s.

Fig. 10 Z (vertical) write disturb test showing that both HRS and LRS of the bottom cell was not disturbed by the BRS at the top cell.
Fig. 11 Superior endurance over $10^{10}$ cycles at both top and bottom cells using a 6 V 1 μs set pulse and a -6.5 V 1 μs reset pulse.

Fig. 12 Negligible degradation of the BRS after $10^{10}$ pulse cycles. The pulse endurance measurement was terminated after $10^{10}$ cycles because of time constrain.

Fig. 13 HRS and LRS currents measured at -2 V as a function of device area. All devices have the same Ti sidewall height of 100 nm but different sidewall lengths.

Fig. 14 Band diagrams of the Ta/TaOx/TiO2/Ti vertical RRAM at (a) set, (b) reset, (c) LRS read at -2 V, (d) HRS read at -2 V, (e) LRS read at +2 V, and (f) HRS read at +2 V. Oxygen ions (O2-) migration in TaOx using Ta as a reservoir is driven by bipolar electric field at set/ reset. The oxygen-vacancy (V2O2-) concentration modulates the Schottky barrier at the Ta/TaOx interface at negative read. Current conduction is dominated by the TaOx/TiO2 barrier at positive read.

Fig. 15 (a) All-line pull-up (All-LPU) read scheme, (b) symmetric 1/3 write scheme, (c) asymmetric 3/4 set - 1/4 reset scheme. Interconnect line resistance of 2.5 Ω/□ was used in the array analysis.

Fig. 16 Read margin of the Ta/TaOx/TiO2/Ti vertical RRAM as a function of array size using the All-LPU read scheme.

Fig. 17 Total read current of the Ta/TaOx/TiO2/Ti vertical RRAM as a function of array size using the All-LPU read scheme.

Fig. 18 Write access voltage at the worse selected bit (normalized to the applied write voltage) as a function of array size using both write schemes in Fig. 15.

Fig. 19 Total write current on the selected BL/WL as a function of array size using both write schemes in Fig. 15. The asymmetric scheme suppresses the sneak current at reset more effectively.

Fig. 20 Worst-case write disturb test at 3/4 $V_{SET}$ shows excellent disturb immunity over 10^3 s at +3.75 V.